This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11 (cancelled)

Claim 12 (currently amended)

A stacked-gate flash memory comprising:

a substrate having a trench formed therein;

a tunneling oxide formed on a surface of said substrate and adjacent to said trench;

a first part of a floating gate formed on said tunneling ~~gate~~ oxide;

a raised isolation filler formed in said trench and protruding over an upper surface of said first part of said floating gate, thereby forming a cavity between two adjacent raised isolation filler;

a second part of said floating gate formed along a surface of said cavity to have U-shaped structure in cross sectional view, wherein the high level of said U-shaped structure is the same with the one of said raised isolation filler;

a dielectric layer conformally formed on a surface of said second part of said floating gate; and

a control gate formed on said dielectric layer.

Claim 13 (original)

The stacked-gate flash memory of Claim 12, wherein said raised isolation filler includes oxide.

Claim 14 (original)

The stacked-gate flash memory of Claim 12, wherein said first part of said floating fate includes polysilicon.